CLAIMS:

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A capacitor forming method comprising:

forming an insulation layer over a substrate, the substrate including an electronic device;

forming a barrier layer to threshold voltage (V_t) shift inducing material over the substrate;

forming an opening at least into the insulation layer;

____forming a high K capacitor dielectric layer at least within the opening; and

providing V_t shift inducing material over the barrier layer, the barrier layer retarding movement of the V_t shift inducing material into the electronic device.

- the insulation layer.
- 3. The method of claim 1 wherein the barrier layer comprises a silicon nitride.
- 4. The method of claim 1 wherein the barrier layer consists essentially of a globally planar barrier layer.
- 5. The method of claim 1 wherein the forming an opening further comprises forming a congruent opening through the barrier layer.

- 6. The method of claim 1 wherein the opening is formed completely through the insulation layer.
- The method of claim 1 wherein the dielectric layer comprises a tantalum oxide.
- 8. The method of claim 1 wherein the providing V_t shift material comprises providing at least one impurity comprising layer over the barrier layer.
- 9. The method of claim 1 wherein the providing V, shift inducing material comprises annealing the dielectric layer.
- 10. The method of claim 9 wherein the annealing comprises oxide annealing.
- ,11. The method of claim 9 wherein the annealing comprises heating the dielectric to at least about 600 °C in the presence of a nitrogen-containing oxide provided at a partial pressure of at least about 200 milliTorr.
- 12. The method of claim 1 wherein the V_t shift inducing material comprises N_2O .

- 13. The method of claim 1 wherein the electronic device comprises a transistor.
- 14. The method of claim 1 wherein the substrate comprises a bulk semiconductor wafer.
- 15. The method of claim 1 further comprising forming a capacitor electrode at least within the opening before forming the dielectric layer.

16. A capacitor forming method comprising:

forming an insulation layer over a substrate, the substrate including an electronic device;

forming a parrier layer to V_t shift inducing material over the insulation layer;

forming an opening through the barrier layer and into the insulation layer;

forming a high K capacitor dielectric layer at least within the opening;

providing V_t shift inducing material over the barrier layer, the barrier layer retarding movement of the V_t shift inducing material into the electronic device.

- 17. The method of claim 16 wherein the barrier layer comprises Si_3N_4 .
- 18. The method of claim 16 wherein the barrier layer consists essentially of a globally planar barrier layer.
- Ta₂O₅. The method of claim 16 wherein the dielectric layer comprises
- The method of claim 16 wherein the providing V_t shift inducing material comprises oxide annealing the dielectric layer and the V_t shift inducing material comprises N_2O .

21. The method of claim 16 further comprising forming a capacitor electrode at least within the opening before forming the dielectric layer.

22. A capacitor forming method/comprising:

forming a barrier layer to V_t shift inducing material over a substrate, the substrate including an electronic device;

forming an insulation layer fover the barrier layer;

forming an opening into at least the insulation layer;

forming a capacitor dielectric layer at least within the opening; and providing V_t shift inducing material over the barrier layer, the barrier layer retarding movement of the V_t shift inducing material into the electronic device.

The method of claim 22 wherein the barrier layer comprises

-24. The method of claim 22 wherein the barrier layer consists essentially of a globally planar barrier layer.

- 25. The method of claim 22 wherein the opening is formed completely through the insulation layer and the barrier layer.
- 26. The method of claim 22 wherein the dielectric layer comprises Ta_2O_5 .
- 27. The method of claim 22 wherein the providing V_t shift inducing material comprises oxide annealing the dielectric layer and the V_t shift inducing material comprises N_2O .

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28. The method of claim 22 further comprising forming a capacitor electrode at least within the opening before forming the dielectric layer.



forming a first insulation layer over a substrate, the substrate including an electronic device;

forming a barrier layer to V_t shift inducing material over the first insulation layer;

forming a second insulation layer over the barrier layer;

forming an opening into at least the second insulation layer;

forming a high K\capacitor dielectric layer at least within the opening;

providing V_t shift inducing material over the barrier layer, the barrier layer retarding movement of the V_t shift inducing material into the electronic device.

- 30. The method of claim 29 wherein the barrier layer comprises Si_3N_4 .
- 31. The method of claim 29 wherein the barrier layer consists essentially of a globally planar barrier layer.
- 32. The method of claim 29 wherein the opening is formed through the second insulation layer and barrier layer and into the first insulation layer.
- 33. The method of claim 29 wherein the dielectric layer comprises Ta_2O_5 .

- The method of claim 29 wherein the providing V_t shift inducing material comprises oxide annealing the dielectric layer and the V_t shift inducing material comprises N_2O .
- 35. The method of claim 29 further comprising forming a capacitor electrode at least within the opening before forming the dielectric layer.

A capacitor forming method comprising:

forming an insulation layer over a substrate, the substrate including an electronic device;

forming an opening into the insulation layer, the opening having a sidewall;

forming a capacitor electrode at least within the opening and over the sidewall;

after forming the apacitor electrode, forming a barrier layer to V_t shift inducing material at least over the insulation-layer;

after forming the barrier layer, forming a high K capacitor dielectric layer at least over the capacitor electrode; and

providing V, shift inducing material over the barrier layer, the barrier layer retarding movement of the V, shift inducing material into the electronic device.

- The method of claim 36 wherein the forming the barrier layer 37. comprises chemical vapor depositing at a step coverage of less than about 25%.
- The method of claim 37 wherein the barrier layer has a .38. thickness over the sidewall of from about 0 to about 300 Angstroms.
- The method of claim 36 wherein the barrier layer comprises 39. Si₃N₄.

40. The method of claim 36 wherein the barrier layer consists essentially of a globally planar barrier layer.

- The method of claim 36 wherein the dielectric layer comprises Ta₂O₅.
- The method of claim 36 wherein the providing V, shift inducing 42. material comprises oxide annealing the dielectric layer and the V_t shift inducing material comprises N₂O.

43. A capacitor forming method comprising:

forming an insulation layer over a substrate, the substrate including an electronic device;

forming an opening into the insulation layer, the opening having a sidewall;

forming a capacitor electrode at least within the opening and over the sidewall;

forming a high K capacitor dielectric layer at least over the capacitor electrode;

after forming the dielectric layer, forming a barrier layer to V_t shift inducing material at least over the insulation layer; and

providing V_t shift inducing material over the barrier layer, the barrier layer retarding movement of the V_t shift inducing material into the electronic device.

44. The method of claim 43 wherein the dielectric layer comprises

comprises chemical vapor depositing at a step coverage of less than about 25%.

46. The method of claim 45 wherein the barrier layer has a thickness over the sidewall of from about 0 to about 300 Angstroms.

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The method of claim 43 wherein the barrier layer comprises Si₃N₄.

- , 48. The method of claim 43 wherein the barrier layer consists essentially of a globally planar barrier layer.
- The method of claim 43 wherein the providing V, shift inducing material comprises oxide annealing the dielectric layer and the Vt shift inducing material comprises N₂O.
- The method of claim 43 wherein the providing V, shift inducing -50. material comprises annealing the dielectric layer and the forming the barrier layer occurs before the annealing....

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an insulation layer over a substrate, the substrate including an electronic device;

a Si_3N_4 barrier layer over the substrate, the barrier layer retarding movement of V_1 shift inducing material into the electronic device;

an opening at least into the insulation layer;

an inner capacitor electrode at least with the opening and comprising silicon;

a high K capacitor dielectric layer at least within the opening and over the inner capacitor electrode; and

an outer capacitor electrode over the dielectric layer.

- 52. The construction of claim 51 wherein the barrier layer is over the insulation layer.
- 53. The construction of claim 51 wherein the barrier layer is under an inner surface of the insulation layer and over the substrate.
- 54. The construction of claim 51 wherein the barrier layer is under an inner surface of the insulation layer and over an outer surface of another insulation layer.
- 55. A semiconductor die comprising the capacitor construction of claim 51.

56. A semiconductor die comprising the capacitor construction of claim 52.

57. A semiconductor die comprising the capacitor construction of claim 53.

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